(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
21 February 2008 (21.02.2008)

PCT

(10) International Publication Number
WO 2008/020819 A1

(51) International Patent Classification:
H01L 33/00 (2006.01)

(21) International Application Number:
PCT/SG2007/000261

(22) International Filing Date: 16 August 2007 (16.08.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
200605500-8 16 August 2006 (16.08.2006) SG

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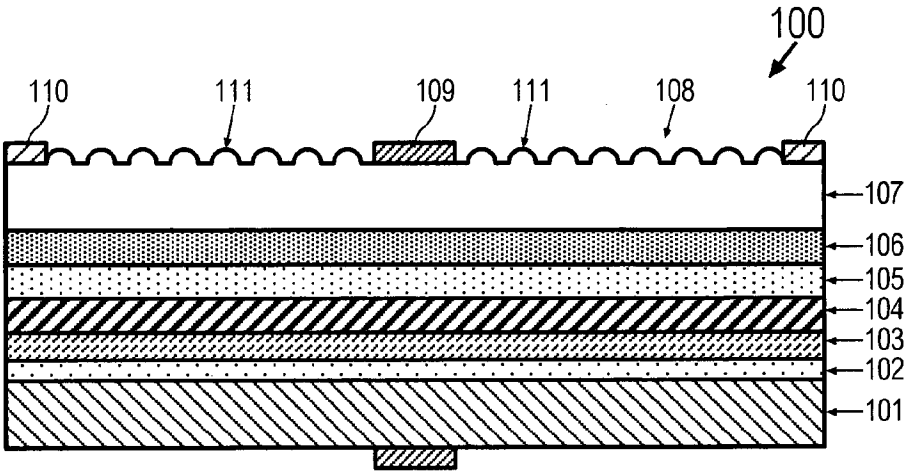
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:
— *of inventorship (Rule 4.17(iv))*

[Continued on next page]

(54) Title: IMPROVEMENTS IN EXTERNAL LIGHT EFFICIENCY OF LIGHT EMITTING DIODES



(57) Abstract: A method to improve the external light efficiency of light emitting diodes, the method comprising etching an external surface of an n-type layer of the light emitting diode to form surface texturing, the surface texturing reducing internal light reflection to increase light output. A corresponding light emitting diode is also disclosed.

WO 2008/020819 A1

Published:
— *with international search report*

Improvements in External Light Efficiency of Light Emitting Diodes

Field of the Invention

This invention relates to improvements in external light efficiency of light emitting diodes and refers particularly, though not exclusively, to light emitting diodes with surface texturing, include micro-lenses and/or surface roughening, on a light output surface, and a method of such surface texturing on a light output surface of light emitting diodes.

Background of the Invention

Ga-N-based light emitting diodes (LEDs) have been intensively studied and developed in recent years. High efficiency, high power, GaN-based LEDs have attracted interest for applications such as displays, traffic signals, back lighting for mobile/cellular telephones and similar apparatus, and white light sources. Reducing cost and improving light output efficiency are important factors to enable such GaN LEDs to succeed in the mainstream lighting market.

In general, the internal quantum efficiency (η_i) for GaN-based LEDs is significantly less than 100% due to crystal quality and epitaxial layer structure. A typical (η_i) can reach about 70 to 80%. Further improvement has proven difficult to achieve. The external quantum efficiency (η_{ext}) is still much lower than internal quantum efficiency. This is because the light extraction efficiency of conventional GaN-based LEDs is limited by total internal light reflection, which occurs at the semiconductor-air interface due to the high refractive index of GaN (n≈2.5) compared to air (n=1). The critical angle for the light generated in the active region is only about 23°. Most of the light generated is repeatedly reflected into the substrate and eventually absorbed. Assuming that light emitted from sidewalls and the bottom is neglected, only a small fraction (4%) can be extracted from the surface.

Conventional GaN-based LEDs grown by metalorganic chemical vapor deposition (MOCVD) use a nonconductive sapphire substrate. The epitaxial layers on the sapphire substrate consists of usually a light-generating layer (active region) sandwiched between a relatively thick n-type doped GaN layer and relatively thin p-type doped GaN layer. The n-type GaN layer is formed by a stack of multiple layers

(undoped or doped to n-type semiconductor made of GaN related materials like GaN, AlGaN, or InGaN, or AlGaInN, etc.) on the sapphire, while the p-type GaN layer is formed by a stack of multiple layers (undoped or doped to p-type semiconductor made of GaN related materials like GaN, AlGaN, or InGaN, or AlGaInN, etc.) away from the sapphire. The top p-GaN surface epitaxial layer is Ga-Polar which is often used as light extraction surface. The poor thermal conductivity of the sapphire substrate, and the relatively high current densities, combine to degrade the device performance due to excessive heating from the active layer during operation. At the same time, the relatively thin p-GaN layer (usually less than 0.5 micrometer) and the high resisitivity of p-GaN, is highly sensitive to plasma damaging and is difficult to use for dry surface texturing. Furthermore, Ga-polar GaN is chemically inert and is more difficult to wet etch than N-polar GaN. The other side of the active region, i.e., the n-GaN layer of the active region is usually much thicker (2 to 5 micrometers thick) than the p-type GaN layer, and is ideal for making surface texturing due to its thickness. However, this part is below the active region and on the sapphire. It is not able to be surface textured unless the sapphire is removed.

To address these problems, vertical laser liftoff of GaN LEDs and other methods have been developed to detach the sapphire from the GaN epitaxial films grown on it. Flip-chip or other bonding technologies have also been developed to attach the GaN films to a new substrate with good thermal conductivity. Different surface roughening techniques on exposed LED N-polar n-GaN surface have also been developed, including ICP plasma etching and wet etching.

The formation of micro-lenses on an output surface of a light emitting diode has been proposed. However, in the main it is not possible as the active region is close to the light emitting surface on the p-type GaN layer and the forming of the micro-lenses or surface roughing may damage the active region.

Summary of the Invention

In accordance with a first preferred aspect there is provided a method to improve the external light efficiency of light emitting diodes, the method comprising etching an external surface of an n-type layer of the light emitting diode to form surface texturing, the surface texturing reducing internal light reflection to increase light output.

According to a second preferred aspect, there is provided a light emitting diode comprising an external surface of an n-type layer of the light emitting diode having surface texturing formed by etching, the surface texturing being for reducing internal light reflection for increasing light output and external light efficiency of the light emitting diode.

According to a third preferred aspect, there is provided a light emitting diode comprising an external surface of an n-type layer of the light emitting diode, and layer of another material being formed on an external surface of the n-type layer, an outermost layer of the layer of another material being surface textured for reducing internal light reflection for increasing light output and external light efficiency of the light emitting diode .

For all aspects the active layer may comprise of one or more of: a quantum well, quantum wells, quantum dots, and quantum wires. The surface texturing may be by wet etching with a chemical solution. The chemical solution may be an aqueous solution of potassium hydroxide at an elevated temperature for a predetermined period. Agitation of the light emitting diode may be used during the etching. The agitation may be by ultraviolet illumination. Additionally or alternatively, the surface texturing may be by dry etching. The dry etching may be plasma etching, plasma bombardment or laser processing. The dry etching may be before or after the wet etching.

The surface texturing may be at least one of: surface roughening, micro-lenses, and surface roughened micro-lenses, holes, voids, pillars and vias. The micro-lenses may be selected from: hemispherical, substantially hemispherical, hemispherical with a flat top, a segment of a sphere, pyramidicial, cylindrical, and cuboid. The micro-lenses may be of:

(a) a spacing between the micro-lenses in the range 2 to 3μm;
(b) a pitch of substantially 6μm; and
(c) a radius of substantially 2μm.

The micro-lenses may be substantially pyramidical and may have facets at an angle of substantially 58°. The surface texturing may be over a part of the external surface. The surface texturing may be in light spaces formed between joining portions and an outer portion of a current dissipation array on the external surface.

A first ohmic contact may be formed on the external surface of the n-type layer and a second ohmic contact may be formed on p-type layer external surface. The second ohmic contact may reflect light for enhancing light emission of the light emitting diode. The second ohmic contact may comprise a stack of multiple layers of metals and their alloys. The metal may be silver, aluminum or another highly reflective metal. The highly reflective metal may be for a light reflection layer for enhancing light reflection of the light emitting diode. The second ohmic contact may cover the entire p-type layer external surface. Alternatively, the second ohmic contact may cover a portion of the p-type layer external surface, with the remainder of the p-type layer external surface being at least partially covered with at least one reflective material for reflecting light for enhancing light emission of the light emitting diode.

The p-type layer, the active layer and the n-type layer may be of one or more of a GaN-related material such as, for example, GaN, InGaN, AlGaN, AlGaInN, InN and AlN.

Surface texturing may also be on the p-type side by surface texturing at least one layer selected from: the p-type layer, the ohmic contact layer, and the contact layer.

Brief Description of the Drawings

In order that the present invention may be fully understood and readily put into practical effect, there shall now be described by way of non-limitative example only preferred embodiments of the present invention, the description being with reference to the accompanying illustrative drawings.

In the drawings:

Figure 1 is a vertical cross-sectional view of a first preferred embodiment;

Figure 2 is an enlarged view of a part of Figure 1;

Figure 3 is an enlarged view of the right-hand end of Figure 2;

Figure 4 is a top plan view of the embodiment of Figure 1;

Figure 5 is a photomicrograph of a portion of a light emitting device according to the first preferred embodiment;

Figure 6 is a scanning electron microscope image of a second preferred embodiment;

Figure 7 is a more detailed image of a portion of Figure 6;

Figure 8 is a graph of L-I characteristics for different etching times;

Figure 9 is a graph of I-V characteristics for different etching times;

Figure 10 is an enlarged side view of a third preferred embodiment;

Figure 11 is an enlarged side view of a fourth preferred embodiment; and

Figure 12 is an enlarged side view of a fifth preferred embodiment.

Detailed Description of the Preferred Embodiments

To refer to Figures 1 to 4 there is shown a first preferred embodiment being a light emitting diode 100 having:

a first contact layer 101 of conductive metal;

a seeding layer 102, a reflective layer 103;

an ohmic contact layer 104;

a p-type material layer 105 such as, for example, GaN;

a plurality of epitaxial layers forming an active layer 106; and

a conductive layer 107 of n-type material such as, for example, GaN.

Any layer may be a stack of multiple layers. The n-type layer 107 is relatively thick, whereas the p-type layer 105 is relatively thin. The active layer 106 may be one or more of: a quantum well, quantum wells, quantum dots and quantum wires.

The conductive layer 107 is for the transmission of light generated in the active layer 106, the light passing through an external light output surface 108 of conductive layer 107. The external surface 108 is the external surface of the air-n-GaN interface. A bonding pad 109 is formed on the external surface 108. A current dissipation array 110 may also be formed on the external surface 108.

The external surface is surface textured to improve external light efficiency by reducing total internal reflection. Surface texturing may be by one or more of surface roughening, micro-lenses, surface roughened micro-lenses, holes, voids, pillars, and vias. One way of surface texturing is to etch the external surface 108 to form a plurality of micro-lenses 111 from external surface 108. The micro-lenses 111 are preferably hemispherical or close to hemispherical. However, they may be of any other suitable shape such as, for example, hemispherical with a flat top, a segment of a sphere, pyramidcial, cylindrical, cuboid, and so forth.

The micro-lenses 111 may be of any suitable size and spacing. For example, the spacing between the micro-lenses 111 may be of the order of 2 or 3μm; the pitch (the spacing between centres of adjacent micro-lenses 111) may be of the order of about 6μm; and each micro-lenses may have a radius of the order of about 2μm.

As shown on Figures 2 and 3, arrows 211, 212 and 213 represent light generated in active layer 106 and passing through layer 107. The majority of the light will pass into micro-lenses 111 or will be incident upon the internal surface 114 of the air/GaN interface. When the angle of incidence of a light beam 211, 212, 213 contacting the internal surface 114 between micro-lenses 111, or the inner surface 113 of micro-lenses 111, at an angle 215 less than the critical angle the light will pass through inner surface 113 and internal surface 114 and will thus be output from the LED 100. If the angle 215 is greater than the critical angle, the light will be reflected by inner surface 113 and internal surface 114. The angle 215 is the angle between the incident light beam 214 and a line 516 perpendicular to a tangent 517 at the point where beam 214 is incident upon surface 113, 114. The critical angle is when angle 215 is such that light beam 214 is reflected by inner surface 113 or internal surface 114 rather than passing through inner surface 113 or internal surface 114 respectively. The critical angle will depend on the material of n-GaN layer 107 and the wavelength of the light 214. If the angle 215 is 0°, the beam 214 will pass through inner surface 113 or internal surface 114 unaffected. If the angle 215 is between the critical angle and 0°, the beam 214 will pass through inner surface 113 or internal surface 114 but may be refracted. A likely range for the angle 215 is 20 to 35°. As noted earlier, for most n-GaN materials and LEDs, the critical angle is about 23°.

Therefore, by controlling the material, size, shape and spacing of micro-lenses 111 it is possible to control the direction and extent of light output from the light emitting diode 100. This may be to the extent that LED 100 could output a focused beam of light.

Figures 4 and 11 show the arrangements of the micro-lenses 111 in a current dissipation array 109, 110 on the external surface 108. The nature, purpose and construction of array 109, 110 is fully disclosed in our co-pending Singapore, patent application number (not yet known) for an invention titled "Electrical Current Distribution in Light Emitting Devices"; the contents of which are incorporated herein by reference as if disclosed herein in its entirety.

The array 109, 110 comprises an outer portion 110 connected to the bonding pad 109 by joining portions 115. Between joining portions 115 and outer portion 110 are a number of light spaces 421, 422, 423 and 424 in which the micro-lenses 111 are located. The light spaces 421, 422, 423 and 424 may each be of substantially the same size and shape, or may different. The number of micro-lenses 111 in each light space 421, 422, 423 and 424, and how they are arrayed, may be the same, or may differ from one light space to the next. A reflective layer 116 may be formed under or within array 109, 110.

The microlens can be formed by etching part of the semiconductor LED. First, photoresist is spun onto the surface, and then patterns are formed on the resist by standard photolithography. These photoresist patterns act as subsequent etching mask for microlens formation. Instead of the photoresist, other materials can also be used as an etching mask. After etching and removal of any residual photoresist, the microlens is formed.

In a second embodiment the surface texturing is surface roughening formed by crystallographic wet etching of all or part of external surface 108. This is by subjecting the n-GaN surface 108 to aqueous potassium hydroxide etching at a temperature such as, for example, room temperature to 200C for a predetermined period. The period may be as small as a few seconds up to several hours. For example, the temperature may be 90°C and the predetermined period may be 7 minutes. The aqueous potassium hydroxide solution may be a 2 Mole potassium hydroxide solution, but other concentrations may be used. Figure 6 shows that the surface 108 is roughened with small grains and Figure 7 shows that the surface morphology of the n-GaN surface 108 displays a high level of roughness at the sub-micron scale with a dense, hexagonal pyramid structure being formed. The facets of the pyramids are in planes inclined at about 58°4°.

Agitation of the light emitting diode may be used during the etching. The agitation may be by ultraviolet illumination. Additionally or alternatively, the surface texturing may be by dry etching. The dry etching may be plasma etching, plasma bombardment or laser processing. The dry etching may be before or after the wet etching.

Such dense nanotip pyramidical structures can be used as nanolenses to increase the light extraction efficiency of GaN-based LEDs. As shown in Figure 7, some of the large pyramids were broken and new small pyramids tips were formed on the top of them. The new, small pyramids grow with time. In such way, the etching of the n-GaN surfaced 108 can continue.

Figure 8 shows the electrical luminescence ("EL") output power from surface 108 versus the injection current (L-I) with different etching times. The data was obtained from the same LED dies before and after KOH wet etching and measured on the wafer before dicing, so that any factor other than the surface morphology could be neglected. The output power at a given current increased significantly after surface roughening. After 7 minutes of KOH etching, the light output power increased by a factor of 2.5 to 3.

Figure 9 shows a comparison of the measured I-V characteristic before and after KOH etching. The degradation of forward voltage drop (V_f) after KOH etching is mainly due to N-metal deterioration. The aluminum inside the Ti/A1/Ti/Au N-metal will slowly deteriorate during KOH etching. This problem may be solved by depositing N-metal after surface roughening. The reverse leakage current does not degrade with the increase of etching time.

Figure 10 shows a third preferred embodiment which is a combination of surface roughening 1001 on the outside surface 112 of micro lenses 111. The surface roughening 1001 may be over all or part of surface 108 and/or all or part of micro lenses 111. In this way the n-GaN surface 108 may have an untreated surface and/or a surface roughened 1001 surface and/or micro lenses 111 and/or micro lenses 111 with surface roughening 1001.

As shown in Figure 12, a layer 1130 of another material may be formed on the external surface 108 of the n-type layer. This may be before or after the surface is surface textured. An outermost surface 1131 of the layer of another material is surface textured for reducing internal light reflection for increasing light output and external light efficiency of the light emitting diode. Surface texturing may be as described above.

The ohmic contact layer 104 is formed on the external surface of the p-type layer 105. The ohmic contact 104 may reflect light for enhancing light emission of the

light emitting diode. The ohmic contact layer 104 may comprise a stack of multiple layers of metals and their alloys. The metal may be silver, aluminum or another highly reflective metal. The highly reflective metal may be for a light reflection layer for enhancing light reflection of the light emitting diode. The second ohmic contact layer 104 may cover the entire external surface of the p-type 105. Alternatively, the ohmic contact layer 104 may cover a portion of the external surface of the p-type layer 105, with the remainder of the external surface of the p-type layer 105 being at least partially covered with at least one reflective material for reflecting light for enhancing light emission of the light emitting diode.

The p-type layer 105, the active layer 106 and the n-type layer 107 may be of one or more of a GaN-related material such as, for example, GaN, InGaN, AlGaN, AlGaInN, InN and AlN.

In addition to the surface texturing on the n-type layer 107, surface texturing may be performed on the p-type side. This may be on p-type layer 105 and/or contact layer 101 and/or ohmic contact layer 104.

Whilst there has been described in the foregoing description preferred embodiments of the present invention, it will be understood by those skilled in the technology concerned that many variations or modifications in details of design or construction may be made without departing from the present invention.

THE CLAIMS

1. A method to improve the external light efficiency of light emitting diodes, the method comprising etching an external surface of an n-type layer of the light emitting diode to form surface texturing, the surface texturing reducing internal light reflection to increase light output.

2. A method as claimed in claim 1, wherein the light emitting diode has a layer of p-type material and an active layer between the n-type layer and the p-type layer.

3. A method as claimed in claim 2, wherein the active layer comprises at least one selected from the group consisting of: a quantum well, quantum wells, quantum dots, and quantum wires.

4. A method as claimed in any one of claims 1 to 3, wherein the surface texturing is by wet etching with a chemical solution.

5. A method as claimed in claim 4, wherein the chemical solution is an aqueous solution of potassium hydroxide and etching is at a temperature for a predetermined period.

6. A method as claimed in any one of claims 1 to 5, wherein agitation of the light emitting diode is performed during the etching.

7. A method as claimed in claim 6, wherein the agitation is by ultraviolet illumination.

8. A method as claimed in any one of claims 1 to 7, wherein the etching is by dry etching.

9. A method as claimed in claim 8, wherein the dry etching is at least one selected from the group consisting of: plasma etching, plasma bombardment or laser processing.

10. A method as claimed in claim 8 or claim 9, wherein the dry etching is before or after the wet etching.

11. A method as claimed in any one of claims 1 to 10, wherein the surface texturing is at least one selected from the group consisting of: surface roughening, micro-lenses, and surface roughened micro-lenses, holes, voids, pillars and vias.

12. A method as claimed in claim 11, wherein the micro-lenses are selected from the group consisting of: hemispherical, substantially hemispherical, hemispherical with a flat top, a segment of a sphere, pyramidicial, cylindrical, and cuboid.

13. A method as claimed in claim 11 or claim 12, wherein the micro-lenses are of:
(a) a spacing between the micro-lenses in the range 2 to 3μm;
(b) a pitch of substantially 6μm; and
(c) a radius of substantially 2μm.

14. A method as claimed in claim 12, wherein the micro-lenses are substantially pyramidical and have facets at an angle of substantially 58°.

15. A method as claimed in any one of claims 1 to 14, wherein the surface texturing is over a part of the external surface.

16. A method as claimed in claim 15, wherein the surface texturing is in light spaces formed between joining portions and an outer portion of a current dissipation array on the external surface.

17. A method as claimed in any one of claims 2 to 16, wherein a first ohmic contact is formed on the external surface of the n-type layer and a second ohmic contact is formed on p-type layer external surface.

18. A method as claimed in claim 17, wherein the second ohmic contact is able to reflect light for enhancing light emission of the light emitting diode.

19. A method as claimed in claim 17 or claim 18, wherein the second ohmic contact comprises a stack of multiple layers of metals and their alloys.

20. A method as claimed in claim 19, wherein the metal is a highly reflective metal including at least one of: silver and aluminum.

21. A method as claimed in claim 20, wherein the highly reflective metal is for a light reflection layer for enhancing light reflection of the light emitting diode.

22. A method as claimed in any one of claims 17 to 21, wherein the second ohmic contact covers the entire p-type layer external surface.

23. A method as claimed in any one of claims 17 to 21, wherein the second ohmic contact covers a portion of the p-type layer external surface, with the remainder of the p-type layer external surface being at least partially covered with at least one reflective material for reflecting light for enhancing light emission of the light emitting diode.

24. A method as claimed in any one of claims 2 to 23, wherein the p-type layer, the active layer and the n-type layer are at least one selected from the group consisting of: a GaN-related material, GaN, InGaN, AlGaN, AlGaInN, InN and AlN.

25. A light emitting diode comprising an external surface of an n-type layer of the light emitting diode having surface texturing formed by etching, the surface texturing being for reducing internal light reflection for increasing light output and external light efficiency of the light emitting diode.

26. A light emitting diode comprising an external surface of an n-type layer of the light emitting diode, and layer of another material being formed on an external surface of the n-type layer, an outermost layer of the layer of another material being surface textured for reducing internal light reflection for increasing light output and external light efficiency of the light emitting diode.

27. A light emitting diode as claimed in claim 25 or claim 26, wherein the light emitting diode has a layer of p-type material and an active layer between the n-type layer and the p-type layer.

28. A light emitting diode as claimed in claim 27, wherein the active layer comprises at least one selected from the group consisting of: a quantum well, quantum wells, quantum dots, and quantum wires.

29. A light emitting diode as claimed in any one of claims 25 to 28, wherein the surface texturing is at least one selected from the group consisting of: surface roughening, micro-lenses, and surface roughened micro-lenses, holes, voids, pillars and vias.

30. A light emitting diode as claimed in claim 29, wherein the micro-lenses are selected from the group consisting of: hemispherical, substantially hemispherical, hemispherical with a flat top, a segment of a sphere, pyramidicial, cylindrical, and cuboid.

31. A light emitting diode as claimed in claim 29 or claim 30, wherein the micro-lenses are of:
(a) a spacing between the micro-lenses in the range 2 to 3μm;
(b) a pitch of substantially 6μm; and
(c) a radius of substantially 2μm.

32. A light emitting diode as claimed in claim 30, wherein the micro-lenses are substantially pyramidical and have facets at an angle of substantially 58°.

33. A light emitting diode as claimed in any one of claims 25 to 32, wherein the surface texturing is over a part of the external surface.

34. A light emitting diode as claimed in claim 33, wherein the surface texturing is in light spaces formed between joining portions and an outer portion of a current dissipation array on the external surface.

35. A light emitting diode as claimed in any one of claims 27 to 34, wherein a first ohmic contact is formed on the external surface of the n-type layer and a second ohmic contact is formed on p-type layer external surface.

36. A light emitting diode as claimed in claim 35, wherein the second ohmic contact is able to reflect light for enhancing light emission of the light emitting diode.

37. A light emitting diode as claimed in claim 35 or claim 36, wherein the second ohmic contact comprises a stack of multiple layers of metals and their alloys.

38. A light emitting diode as claimed in claim 37, wherein the metal is a highly reflective metal including at least one of: silver and aluminum.

39. A light emitting diode as claimed in claim 38, wherein the highly reflective metal is for a light reflection layer for enhancing light reflection of the light emitting diode.

40. A light emitting diode as claimed in any one of claims 35 to 39, wherein the second ohmic contact covers the entire p-type layer external surface.

41. A light emitting diode as claimed in any one of claims 35 to 39, wherein the second ohmic contact covers a portion of the p-type layer external surface, with the remainder of the p-type layer external surface being at least partially covered with at least one reflective material for reflecting light for enhancing light emission of the light emitting diode.

42. A light emitting diode as claimed in any one of claims 27 to 41, wherein the p-type layer, the active layer and the n-type layer are at least one selected from the group consisting of: a GaN-related material, GaN, InGaN, AlGaN, AlGaInN, InN and AlN.

43. A light emitting diode as claimed in any one of claims 25 to 42 further comprising surface texturing on the p-type side.

44. A light emitting diode as claimed in claim 43, wherein the surface texturing on the p-type side is on at least one layer selected from the group consisting of: the p-type layer, the ohmic contact layer, and the contact layer.

45. A method as claimed in any one of claims 1 to 24 further comprising surface texturing on the p-type side by surface texturing at least one layer selected from the group consisting of: the p-type layer, the ohmic contact layer, and the contact layer.

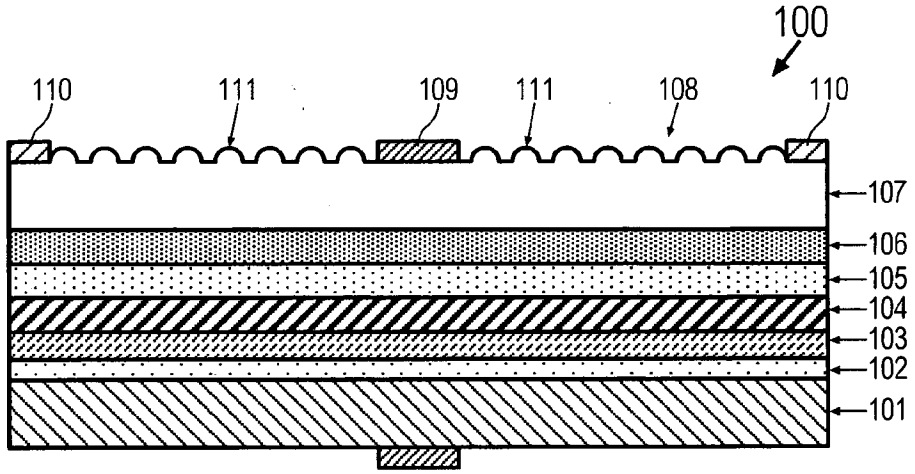


FIG. 1

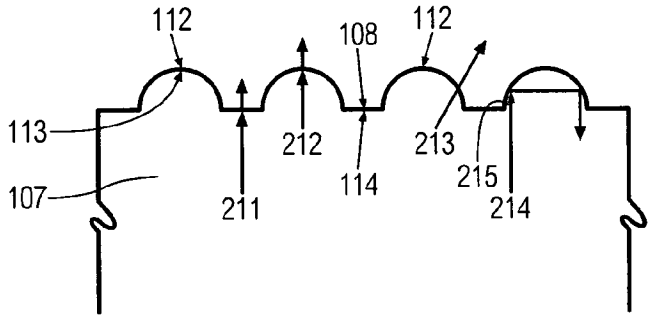


FIG. 2

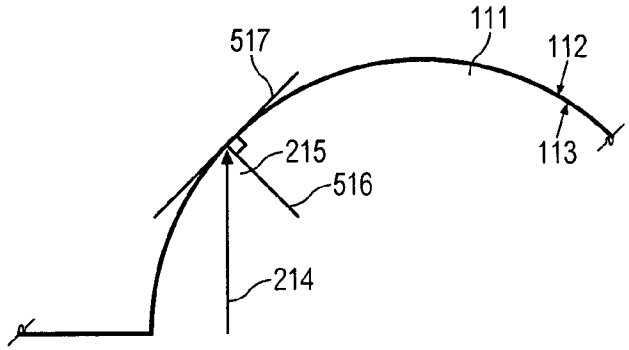


FIG. 3

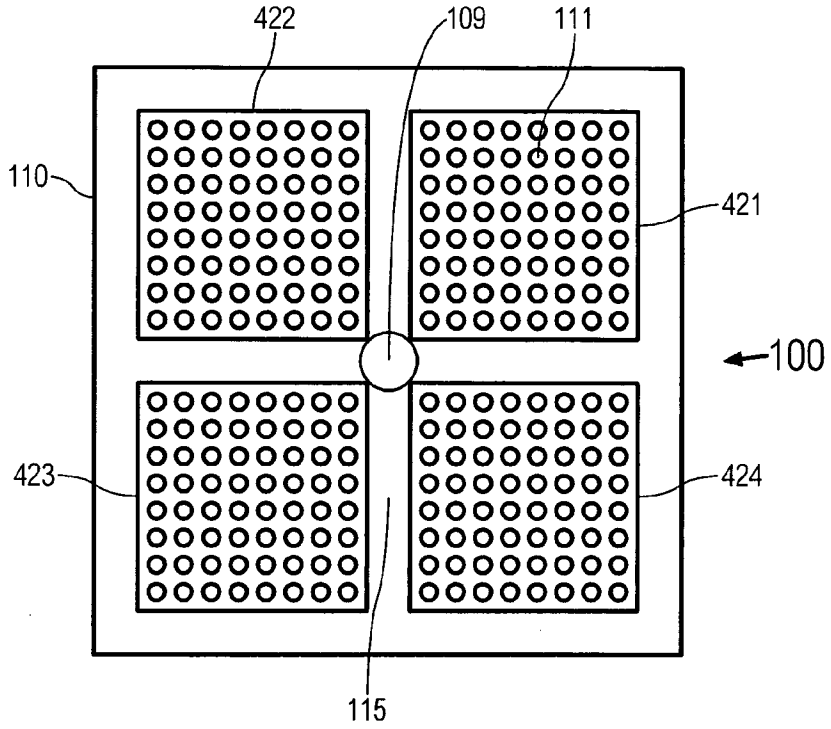


FIG. 4

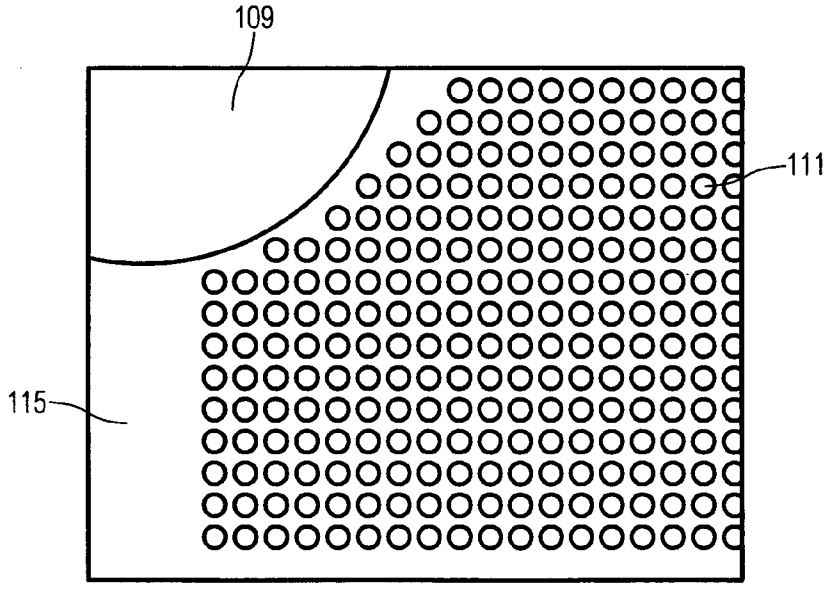


FIG. 5

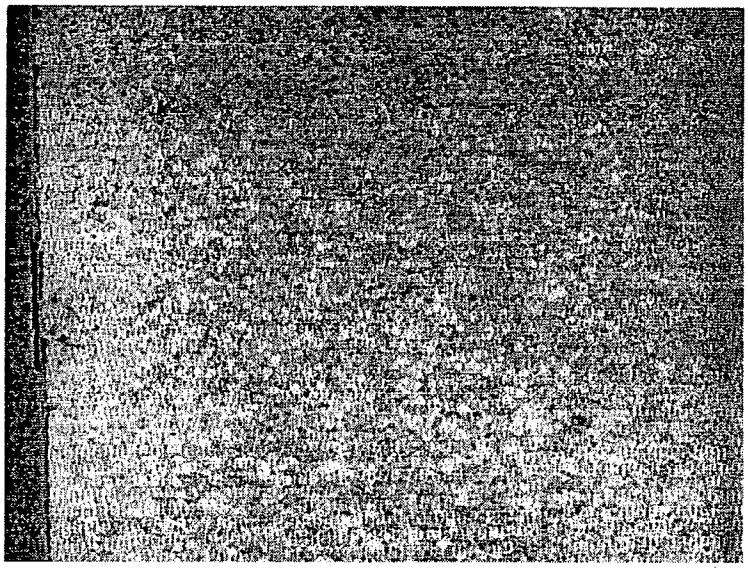


FIG. 6

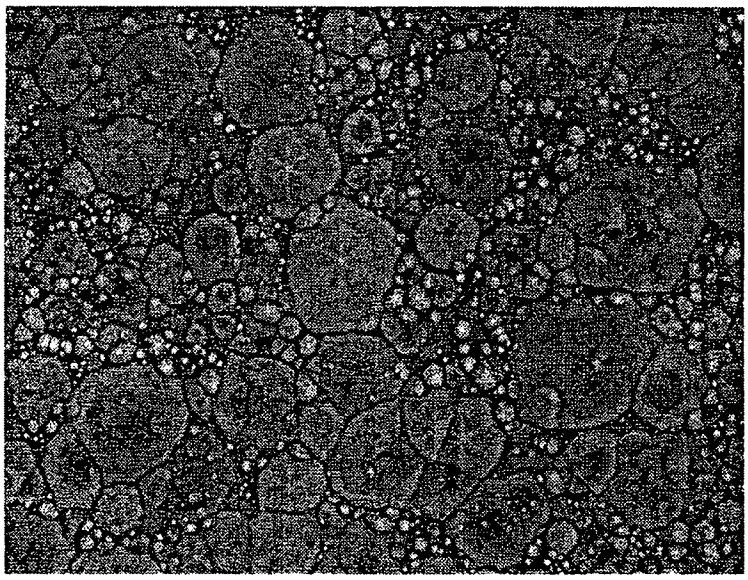


FIG. 7

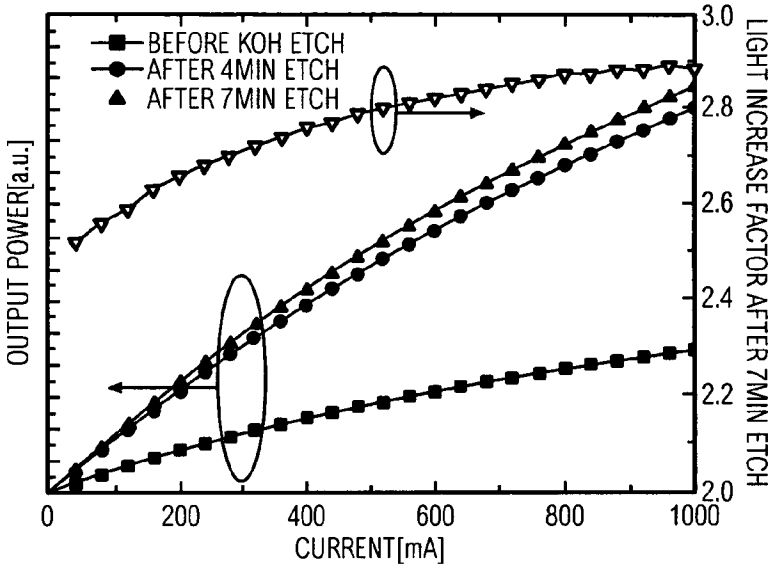

BEFORE KOH ETCH
AFTER 4MIN ETCH
AFTER 7MIN ETCH
OUTPUT POWER[a.u.]
LIGHT INCREASE FACTOR AFTER 7MIN ETCH
CURRENT[mA]
0
200
400
600
800
1000
2.0
2.2
2.4
2.6
2.8
3.0

FIG. 8

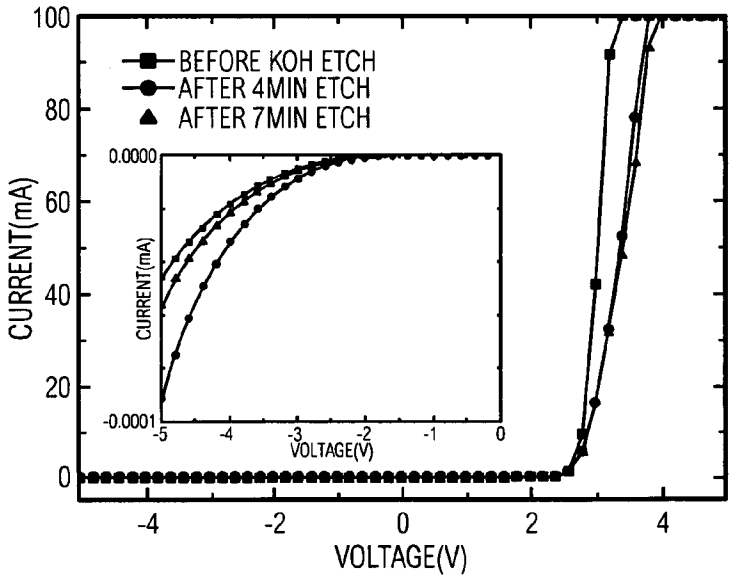

BEFORE KOH ETCH
AFTER 4MIN ETCH
AFTER 7MIN ETCH
CURRENT(mA)
VOLTAGE(V)
0.0000
-0.0001
-5
-4
-3
-2
-1
0
100
80
60
40
20
0
-4
-2
0
2
4

FIG. 9

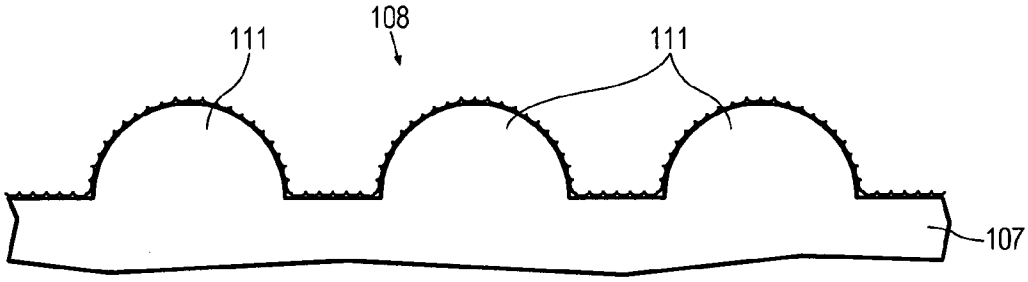


FIG. 10

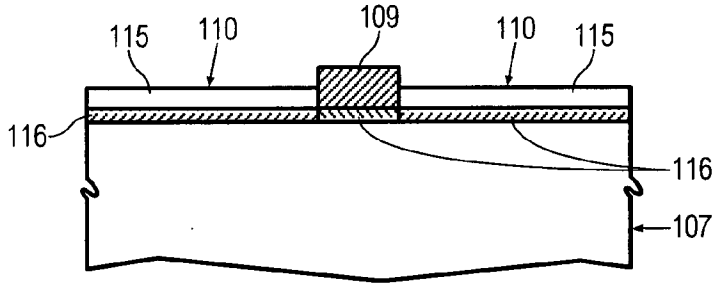


FIG. 11

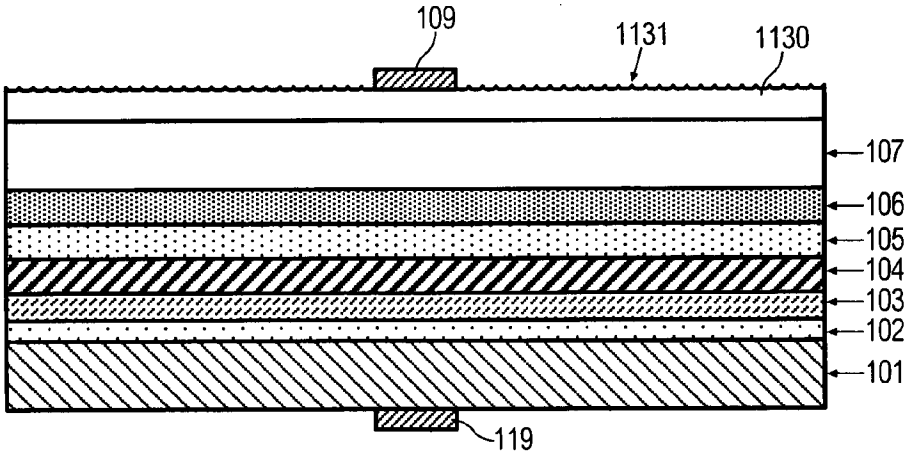


FIG. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2007/000261

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.

H01L 33/00 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
DWPI AND JAPIO: (led? or (light (1d)diode?)) and ((texture+ or pattern+ or etch+ or rough+)(s)(surfac+ or outer or exterior or top or external+ or outside)) and ((n-type) or (n(1d)type+) or (dop+(d)n)) and ((increas+ or rais+ or improv+ or maximi+)(s)(light+ or effici+ or emission+ or transmiss+)) and ((reduce+ or lower+ or minimi+) (s) (reflection))

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	Patent Abstracts of Japan, JP 2005-236048 A (SHIN ETSU HANDOTAI CO LTD) 2 September 2005	26,27,29,33
X	EP 1 061 590 A1 (SHIN-ETSU HANDOTAI CO LTD) 20 December 2000 See paras 0027 and 0031 and fig 1.	1,2,4,11,15,17 ,25-27,29,33, 35,43,44,45
X	Patent Abstracts of Japan, JP 2006-253647 A (ROHM CO LTD) 21 September 2006	1,2,11,15, 17,25
X	Patent Abstracts of Japan, JP 2001-036129 A (DOWA MINING CO LTD) 9February 2001	1,2,11,15,17, 22,25-27,29, 33,40,43-45

[X] Further documents are listed in the continuation of Box C [X] See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
03 October 2007	12 OCT 2007
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. (02) 6285 3929	Authorized officer **S. T. PRING** AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No : (02) 6283 2210

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2007/000261

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	Derwent Abstract Accession No. 2003-056533/05, Class L03, TW 475276 A (IND TECHNOLOGY RES INST)	1,2,11,15,17, 18,24,25,27, 29,33
X	Derwent Abstract Accession No. 2003-694325/66, Class L03, KR 2002-079659 A (EPIVALLEY CO LTD) 19 October 2002	1,11,15, 17,24,25
P,X	US 2007/0029541 A1 (XIN et al) 8 February 2007 See para 0048 and para 0049 and figs 3,5.	1,4,8,9,11,15, 25,29,33
P,X	US 2006/0186418 A1 (EDMOND et al) 24 August 2006 See paras 0024,0037,0038,0040.	1,4-7,11,15, 17,22,24,25, 27,29,33
X	US 2005/0014303 A1 (TSAI et al) 20 January 2005 See paras 0030, 0033 and fig 2c.	26,29,30, 33,42-45
X	US 2006/0163586 A1 (DENBAARS et al) 27 July 2006 See paras 0038, 0041, and 0044.	1,2,4,11,15, 17,24-27,29, 33,35,42
X	US 2006/0124939 A1 (LEE et al) 15 Jun 2006 See fig 4 and para 0073	1,2,4-9,11,17,24-27,29,35,42
X	WO 2005/064666 A1 (THE REGENTS OF THE UNIVERSITY OF CALIFORNIA) 14 July 2005 See abstract and page 11 lines 1-11, claims 12,14, page 7 lines 9-15.	1,2,4-12,14-18,24-27,29, 30,32-36,42

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/SG2007/000261

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
JP	2005236048	CN	1658406				
EP	1061590	JP	2000196141	WO	0041249		
JP	2006253647	WO	2006085514				
JP	2001036129		NONE				
TW	475276		NONE				
KR	2002079659		NONE				
US	2007029541		NONE				
US	2006186418	CA	2564995	CN	1957481	EP	1763900
		KR	2007001332	US	2006049411	WO	2005117152
		WO	2007089460				
US	2005014303	US	6921924	US	2004256627		
US	2006163586	WO	2006080958				
US	2006124939	KR	2006006661	KR	2006006662	US	2006124941
		WO	2006065010	WO	2006065046		
WO	2005064666	AU	2003296426	CN	1886827	EP	1697983
		US	2007121690				

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX